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10/602,436	06/23/2003	Jong-Jan Lee	SLA 0733	9661

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,436	LEE ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sh t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 25 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In Claim 25, Applicant recites that the *"first silicon containing layer is a silicon layer,"* and the second is a "*silicon germanium layer.*" Claims 25 and 26 are dependent upon Claim 12. However, Claim 12 recites that the channel layer (second layer) has a lattice constant smaller than that of the seed fin (first) layer. Since silicon has a smaller lattice constant than silicon germanium (See Specification, p.12, lines 14 – 16), the second layer of Claim 25 has a larger lattice constant than the first, contradicting Claim 12. Hence, the limitations are contradictory and not definitive. Correction is required.

Claim Rejections – 35 U.S.C. 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application

filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 12 – 17, 19, 21 – 23, 27, 30, 31, 33, 34, 37, 38, and 40 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (US 6,800,910 B2).

5. Regarding Claim 12, Lin et al. disclose a method of fabricating a strained silicon finFET device, comprising the steps of:

providing a silicon on insulator (SOI) substrate (Col. 4, line 27) having a silicon containing multilayer (42) (Figure 4a) on an insulator layer (40) (Col. 4, lines 27 – 28),

patterning the multilayer into a source region and a drain region (82) (Figure 7) sandwiching a seed channel region (82), the seed channel being a seed fin structure (48) (Figure 4c),

depositing an epitaxial channel layer (Col. 4, lines 43 – 44) onto the seed fin structure (48), the channel layer material (Si) having a lattice constant smaller than that of the seed fin material (SiGe) wherein the epitaxial channel layer becomes a tensile strained channel layer due to lattice mismatch between channel layer and seed fin structure (Col. 3, lines 44 – 60),

forming a gate dielectric layer (Col. 4, lines 55 – 57) on the epitaxial strained channel, and

forming a gate (48) (Figure 4c) over the epitaxial strained channel (Col. 4, lines 64 – 65).

6. Regarding Claim 13, Lin et al. disclose that the silicon containing multilayer comprises

silicon (Col. 4, lines 28 – 29).

7. Regarding Claim 14, Lin et al. disclose a method wherein the silicon on insulator substrate is an SGOI substrate (Col. 2, lines 16 – 18) wherein the silicon containing multilayer comprises a silicon germanium layer (42) (Figure 4a) (Col. 4, lines 28 – 29).

8. Regarding Claim 15, Lin et al. disclose a method wherein the germanium content of the silicon germanium seed fin is between 10% and 100 % (Col. 4, lines 31 – 33).

9. Regarding Claim 16, Lin et al. disclose that the epitaxial channel layer is a silicon layer (Col. 4, lines 43 – 44).

10. Regarding Claim 17, Lin et al. disclose that conventional lithographic processes are used in patterning and defining channel and adjacent source/drain regions (Figure 7) (80, 82), whereinafter, the mask is removed to yield the structure shown in Figure 4c.

11. Regarding Claim 19, Lin et al. disclose that formation of the gate comprises the steps of:

depositing a gate material layer (48) (Figure 4c),

patterning and defining the gate, as discussed above, using conventional lithographic processes and subsequently removing mask.

Lin et al. do not explicitly disclose that the gate material is doped. Lin et al. do disclose that

the gate material is formed of polysilicon (Col. 4, lines 65 – 67). It is known that as-deposited polysilicon is relatively non-conducting. In order for the polysilicon to function as a conducting gate, the material would require doping. It is therefore inherent that the gate material is doped.

12. Regarding Claim 21, Lin et al. disclose a method further comprising:

forming dielectric spacers between the gate and the source and drain regions (Col. 5, lines 5 – 6),

doping the source/drain regions (Col. 5, lines 6 – 7), and

forming silicide of the gate, source, and drain regions (Col. 5, lines 7 – 8).

13. Regarding Claim 22, Lin et al. disclose that the multilayer comprises:

a first silicon-containing layer (42) (Figure 4a) (Col. 4, lines 28 – 29), and

a second silicon-containing layer (46) (Figure 4b) having a lattice constant different that that of the first material, wherein the second layer becomes a strained layer (Col. 4, lines 43 – 44) due to lattice mismatch between channel layer and the first layer.

14. Regarding Claim 23, Lin et al. disclose that the multilayer is formed by providing a silicon on insulator (SOI) substrate (Col. 1, lines 35 – 44) having a first silicon containing layer (42) (Figure 4a) on an insulator layer (42) (Col. 4, lines 28 – 29), depositing a second silicon containing layer material (46) wherein the lattice constant of the second silicon containing material is different from that of the first silicon containing layer.

15. Regarding Claim 27, Lin et al. disclose that the top most layer of the multilayer (44) comprises a hard mask layer (Col. 4, lines 34 – 38).

16. Regarding Claim 30, Lin et al. disclose that the thickness of the strained channel layer is 80 Angstroms (8nm) to 200 Angstroms (20nm), consistent with the recitations of the instant application.

17. Regarding Claim 31, Lin et al. disclose a method of fabricating a strained silicon finFET device, comprising the steps of:

providing a silicon on insulator (SOI) substrate (Col. 4, lines 26 – 27), the silicon on insulator substrate comprising a relaxed silicon germanium layer on an insulator layer,

patterning the relaxed silicon germanium layer into a source region and a drain region (82) (Figure 7) sandwiching a seed channel region (82), the seed channel being a seed fin structure (48) (Figure 4c),

depositing an epitaxial channel layer (Col. 4, lines 43 – 44) onto the seed fin structure (48), wherein the epitaxial channel layer becomes a tensile strained channel layer due to lattice mismatch between channel layer and seed fin structure (Col. 3, lines 44 – 60),

forming a gate dielectric layer (Col. 4, lines 55 – 57) on the epitaxial strained silicon channel, and

forming a gate (48) (Figure 4c) over the epitaxial strained silicon channel (Col. 4, lines 64 – 65).

18. Regarding Claims 33, 37, and 40, Lin et al. disclose a method comprising:

depositing a hard mask layer (44) onto the relaxed silicon germanium layer (Col. 4, lines 34 – 38),

wherein the deposited hardmask layer is also patterned together with the silicon germanium layer (Col. 4, lines 39 – 42).

19. Regarding Claim 34, Lin et al. disclose a method of fabricating a strained silicon FINFET device, comprising the steps of:

providing a silicon on insulator substrate comprising a silicon (semiconductor) layer on an insulator layer (Col. 6, lines 58 – 61),

depositing a silicon germanium layer onto the silicon (semiconductor) layer (Col. 6, lines 58 – 61),

patterning the multilayer into a source region and a drain region (82) (Figure 7) sandwiching a seed channel region (82), the seed channel being a seed fin structure (48) (Figure 4c),

depositing an epitaxial channel layer (Col. 4, lines 43 – 44) onto the seed fin structure (48), the channel layer material (Si) having a lattice constant different that that of the seed fin material (SiGe) wherein the epitaxial channel layer becomes a tensile strained channel layer due to lattice mismatch between channel layer and seed fin structure (Col. 3, lines 44 – 60),

forming a gate dielectric layer (Col. 4, lines 55 – 57) on the epitaxial strained channel, and

forming a gate (48) (Figure 4c) over the epitaxial strained channel (Col. 4, lines 64 – 65).

20. Regarding Claim 38, Lin et al. disclose a method of fabricating a strained silicon FINFET device, comprising:

providing a silicon on insulator (SOI) substrate (Col. 4, lines 26 – 27), the silicon on insulator substrate comprising a relaxed silicon germanium layer on an insulator layer,

depositing an epitaxial silicon channel layer (Col. 4, lines 43 – 44) onto the seed fin structure (48), wherein the epitaxial silicon channel layer becomes a tensile strained silicon channel layer due to lattice mismatch between channel layer and seed fin structure (Col. 3, lines 44 – 60),

patterning the multilayer of epitaxial silicon channel layer and silicon germanium layer into a source region and a drain region (82) (Figure 7) sandwiching a seed channel region (82), the seed channel being a seed fin structure (48) (Figure 4c),

forming a gate dielectric layer (Col. 4, lines 55 – 57) on the epitaxial strained silicon channel, and

forming a gate (48) (Figure 4c) over the epitaxial strained silicon channel (Col. 4, lines 64 – 65).

Claim Rejections – 35 U.S.C. 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art

are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., as applied to Claims12 – 17, 19, 21 – 23, 27, 30, 31, 33, 34, 37, 38, and 40, and further in view of Wolf et al. ("Silicon Processing for the VLSI Era, Volume 1 – Process Technology," Lattice Press, Sunset Beach, CA (1986).

23. Regarding Claim 18, Lin et al. do not disclose doping of the channel region. However, doping of the channel region is notoriously well known and done for decades to adjust the threshold voltage (See for example, Wolf et al., p. 325, top of page). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wolf et al. with Lin et al. to provide a FET device of improved efficiency.

24. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., as applied to Claims 12 – 17, 19, 21 – 23, 27, 30, 31, 33, 34, 37, 38, and 40, and further in view of Pham et al. (US 6,838,322 B2).

25. Regarding Claim 20, Lin et al. do not disclose the formation of lightly doped drain (LDD) and halo regions between the channel and source and drain regions. Pham et al. daisclose for a FINFET device the formation of LDD or extension regions (Col. 6, lines 20 – 22). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Pham et al. with Lin et al. to reduce short channel effects in the FINFET device.

26. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) overLin et al., as applied to Claims 12 – 17, 19, 21 – 23, 27, 30, 31, 33, 34, 37, 38, and 40, and further in view of Dakshina-Murthy et al. (US 6,803,631 B2).

27. Regarding Claim 28, Lin et al. do not disclose the height of the seed fin structure. Dakshina-Murthy et al. disclose for a strained channel FINFET that the fin structure (formed from the deposited layer 105) (Col. 3, lines 14 – 16) height (205) (Figure 2A) is from about 500 Angstroms (50 nm) to about 1000 Angstroms (100 nm), well within the range recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Dakshina-Murthy et al. with Lin et al. to obtain a FINFET structure compatible with higher packing densities (Dakshina-Murthy et al., Col.1, lines 25 – 27).

28. Regarding Claim 29, Lin et al. do not disclose the width of the seed fin structure. Dakshina-Murthy et al. disclose for a strained channel FINFET that the width of the fin structure is in the range, 10 to 15 nm, within the range recited in the instant application. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Dakshina-Murthy et al. with Lin et al. to obtain a FINFET structure compatible with higher packing densities (Dakshina-Murthy et al., Col.1, lines 25 – 27).

29. Claims 32 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., as appllied to Claims 12 – 17, 19, 21 – 23, 27, 30, 31, 33, 34, 37, 38, and 40, and further

in view of Chu et al. (6,350,993 B1).

30. Regarding Claims 32 and 36, Lin et al. do not disclose that the deposited epitaxial silicon channel layer comprises a germanium component to form a tensile strained silicon germanium strained channel layer on the seed fin structure, with the germanium composition of the channel layer being less than that of the underlying silicon germanium layer. Chu et al. disclose a layered SiGe heterostructure in which the top layers (17,18) in the channel region (Figures 1 and 12) wherein the germanium concentration of layer 17 is 80 % (Col. 8, lines 4 – 6) and 35 % for layer 18 (Col.8, lines 16 – 20), such that the germanium concentration in the underlayer is higher than that of the (top) SiGe layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Chu et al. with Lin et al. to obtain a device with improved mobility values.

31. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., as applied to Claims12 – 17, 19, 21 – 23, 27, 30, 31, 33, 34, 37, 38, and 40, and further in view of Murakami et al. (US 5,241,197).

32. Regarding Claim 35, Lin et al. do not disclose that the deposited epitaxial silicon channel layer comprises a germanium component to form a silicon germanium layer on the substrate, the germanium concentration of the silicon germanium layer being less than that of the subsequently deposited silicon germanium layer. Murakami et al. disclose an FET transistor structure (Figure 8) with multiple layers, wherein the films 85 and 22 are Ge films (100%

concentration) formed onto a SiGe film (311) where the Ge concentration is 50%, such that the Ge concentration of the silicon germanium layer on insulator is less than the subsequently deposited silicon germanium layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Murakami et al. with Lin et al. to obtain a device with improved mobility values.

33. Claim 41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Candelaria (US 5,441,901).

34. Regarding Claim 41, Lin et al. disclose a method of fabricating a strained silicon FINFET device, comprising:

providing a silicon on insulator substrate comprising a silicon (semiconductor) layer on an insulator layer (Col. 6, lines 58 – 61),

patterning the multilayer into a source region and a drain region (82) (Figure 7) sandwiching a seed channel region (82), the seed channel being a seed fin structure (48) (Figure 4c),

forming a gate dielectric layer (Col. 4, lines 55 – 57) on the epitaxial strained channel, and

forming a gate (48) (Figure 4c) over the epitaxial strained channel (Col. 4, lines 64 – 65).

Lin et al. do not disclose the deposition of an epitaxial carbon doped silicon channel layer onto the fin structure, wherein the epitaxial silicon carbon layer becomes a tensile strained

silicon channel layer due to mismatch between silicon carbon and silicon. Candelaria discloses the deposition of an epitaxial carbon doped layer (44) onto silicon (43) (Figure 4) for a heterojunction device (Col. 5, lines 45 – 47). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the epitaxial layer deposition of carbon doped silicon of Candelaria in Lin et al to obtain a tensile strained silicon channel layer due to lattice mismatch (Lin et al., Col. 6, lines 64 – 66).

35. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., as applied to Claims 12 – 17, 19, 21 – 23, 27, 30, 31, 33, 34, 37, 38, and 40, and further in view of Yu (US 6,475,869 B1).

36. Regarding Claim 24, Lin et al. do not disclose that the thickness of the first silicon containing region is between 5 to 20 nm. Yu discloses a thickness (width) between 5 to 20 nm. (Figures 4 – 6) (Col. 5, lines 37, 44). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yu and Lin et al. to obtain a FINFET device with high driving current (Lin et al., Col. 1, lines 63 – 67).

Response to Arguments

37.. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusions

38. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
January 16, 2005

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